

Abstracts

GSM 900/DCS 1800 fractional-N modulator with two-point-modulation

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This paper presents a fractional-N modulator architecture that uses the technique of two-point-modulation. This technique allows direct modulation of the VCO within the closed loop of a high resolution PLL based fractional-N frequency synthesizer, without restriction due to loop bandwidth and PLL dynamics. A prototype transmitter was implemented using the GSM standard to verify the superior performance predicted by simulation. The core element of this new modulator architecture is a PLL-based fractional-N frequency synthesizer. This prototype synthesizer consists essentially of a full custom IC for the analog section, and the digital functionality was implemented in a field programmable gate array (FPGA). The analog circuitry was fabricated in a 25 GHz BiCMOS process with 0.8 μ m as minimum feature size. Measurements of the spectrum for the GSM modulated signal and of the demodulated signal show that the strict demands of the GSM specification can be met.

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